

## 80V N-Ch Power MOSFET

### Feature

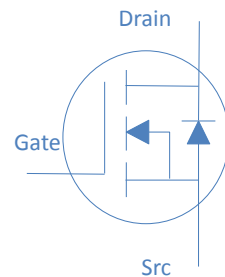
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free

$V_{DS}$		80	V
$R_{DS(on),typ}$	$V_{GS}=10V$	4.3	m $\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	5.9	m $\Omega$
$I_D$ (Silicon Limited)		100	A
$I_D$ (Package Limited)		60	A

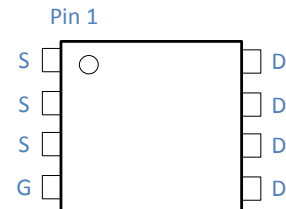
### Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control

DFN5x6



Part Number	Package	Marking
HGN058N08SL	DFN5*6	GN058N08SL



### Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ\text{C}$	100	A
		$T_C=100^\circ\text{C}$	63	
		Continuous Drain Current (Package Limited)	$T_C=25^\circ\text{C}$	
Drain to Source Voltage	$V_{DS}$		-	80
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	350	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.3\text{mH}, T_C=25^\circ\text{C}$	240	mJ
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	104	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	$^\circ\text{C}$

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.2	$^\circ\text{C/W}$
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

**Electrical Characteristics at T<sub>J</sub>=25°C (unless otherwise specified)**
**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	80	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	1	1.7	2.4	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =80V, T <sub>J</sub> =25°C	-	-	1	μA
		V <sub>GS</sub> =0V, V <sub>DS</sub> =80V, T <sub>J</sub> =100°C	-	-	100	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Drain to Source on Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	4.3	5.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	5.9	8.0	mΩ
Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	65	-	S
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> Open, f=1MHz	-	1.5	-	Ω

**Dynamic Characteristics**

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =40V, f=1MHz	-	3130	-	pF
Output Capacitance	C <sub>oss</sub>		-	385	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	18	-	
Total Gate Charge (10V)	Q <sub>g</sub> (10V)	V <sub>DD</sub> =40V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	46	-	nC
Total Gate Charge (4.5V)	Q <sub>g</sub> (4.5V)		-	22	-	
Gate to Source Charge	Q <sub>gs</sub>		-	9	-	
Gate to Drain (Miller) Charge	Q <sub>gd</sub>		-	8	-	
Turn on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =40V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>G</sub> =10Ω,	-	11	-	ns
Rise time	t <sub>r</sub>		-	7	-	
Turn off Delay Time	t <sub>d(off)</sub>		-	38	-	
Fall Time	t <sub>f</sub>		-	9	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>F</sub> =20A	-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>R</sub> =40V, I <sub>F</sub> =20A, dI <sub>F</sub> /dt=400A/μs	-	48	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>		-	190	-	nC

Fig 1. Typical Output Characteristics

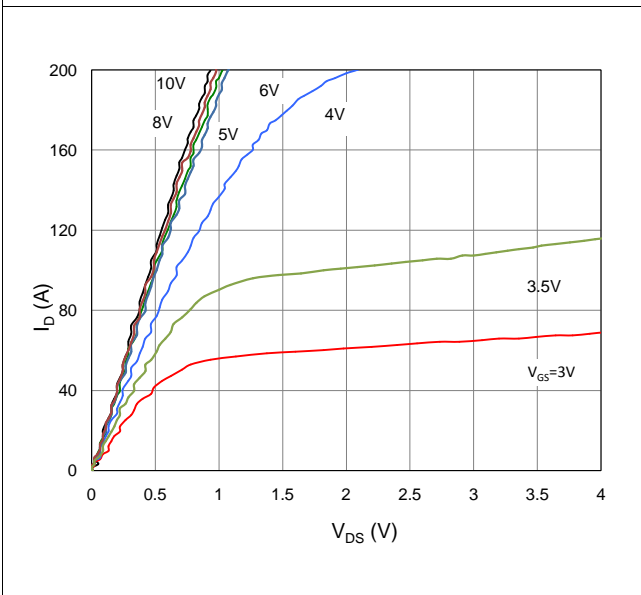


Figure 2. On-Resistance vs. Gate-Source Voltage

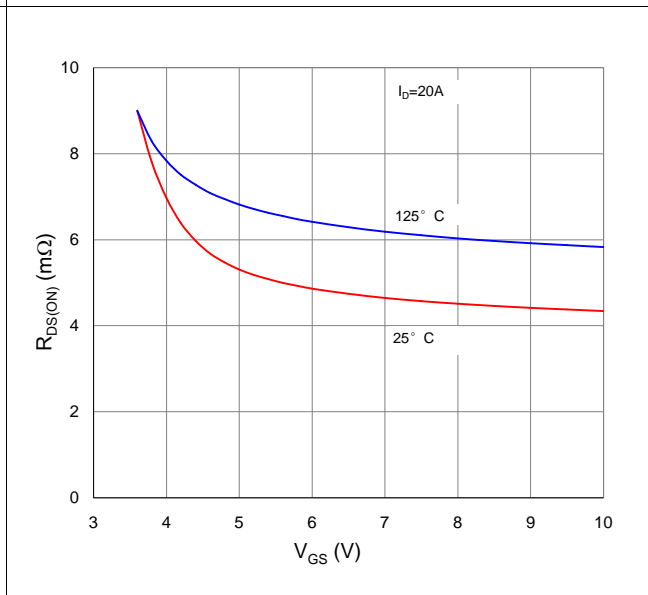


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

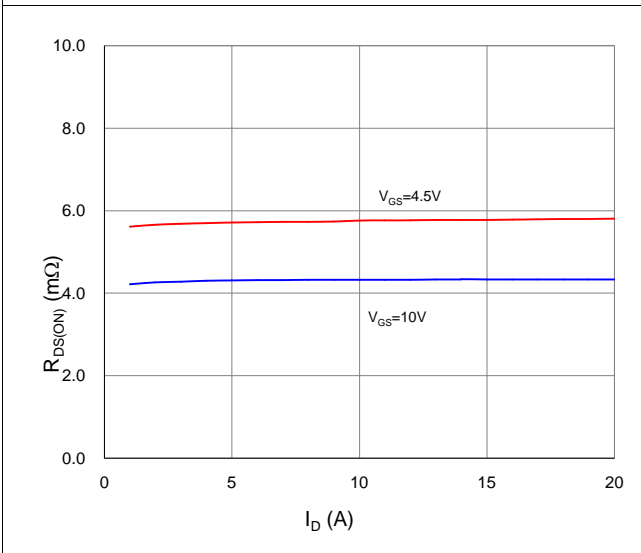


Figure 4. Normalized On-Resistance vs. Junction Temperature

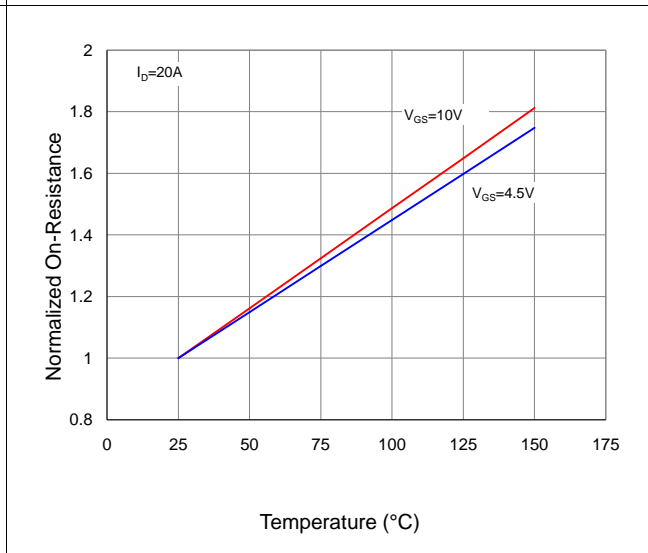


Figure 5. Typical Transfer Characteristics

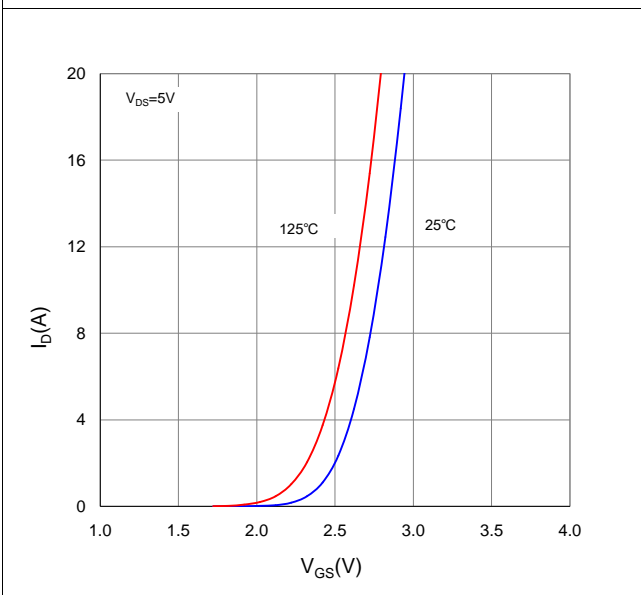


Figure 6. Typical Source-Drain Diode Forward Voltage

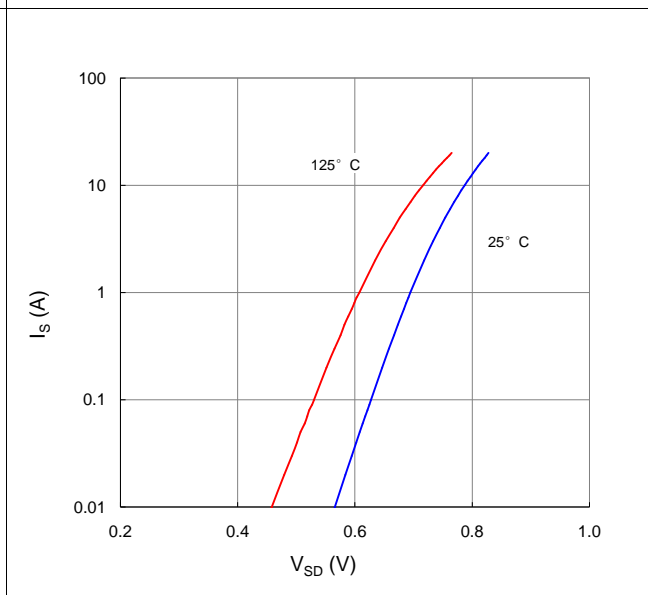


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

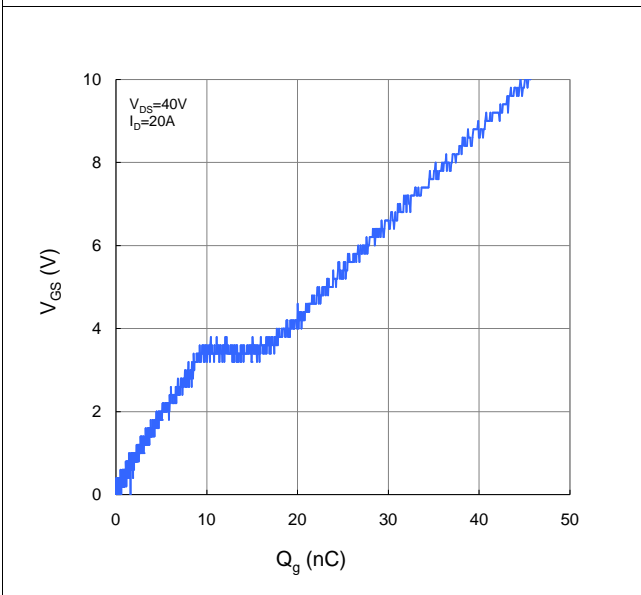


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

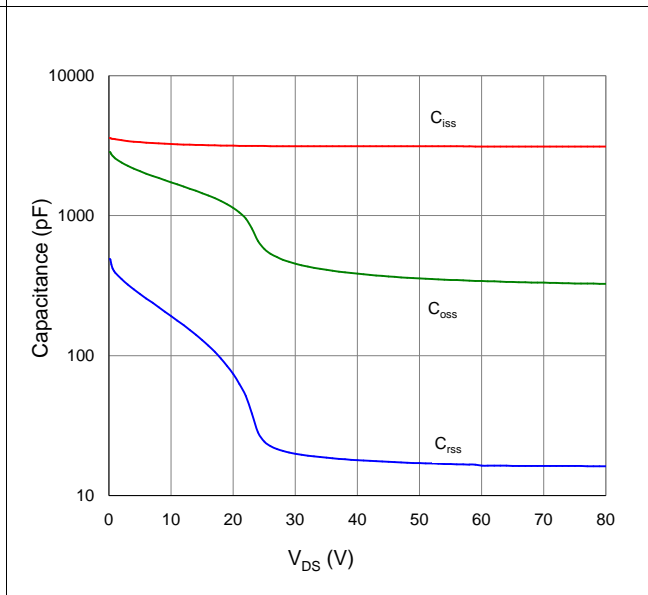


Figure 9. Maximum Safe Operating Area

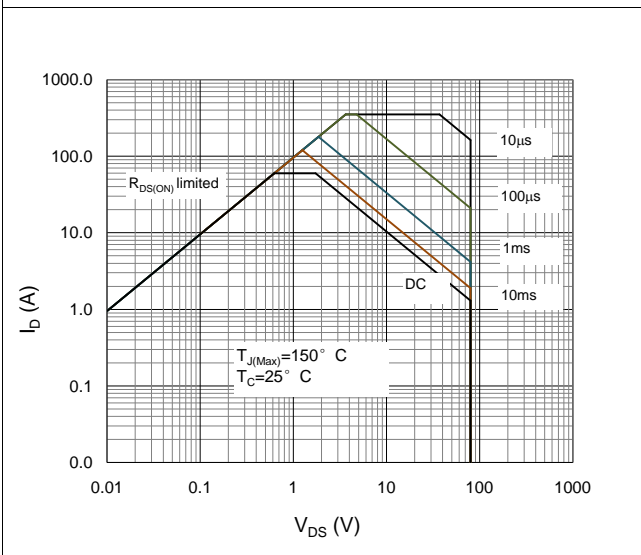


Figure 10. Maximum Drain Current vs. Case Temperature

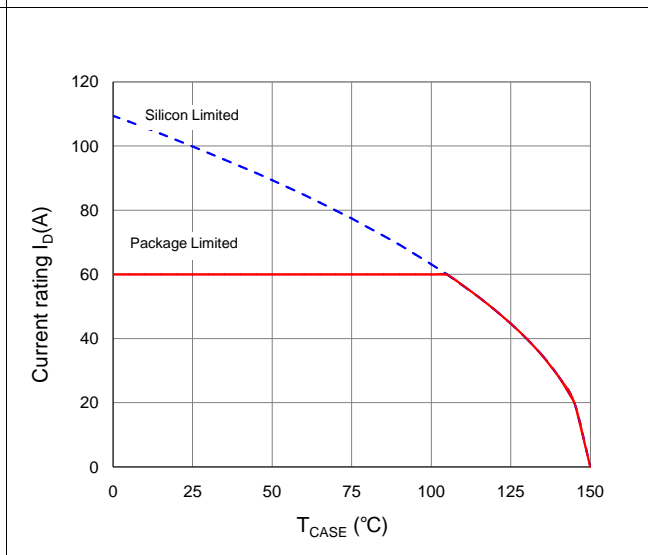
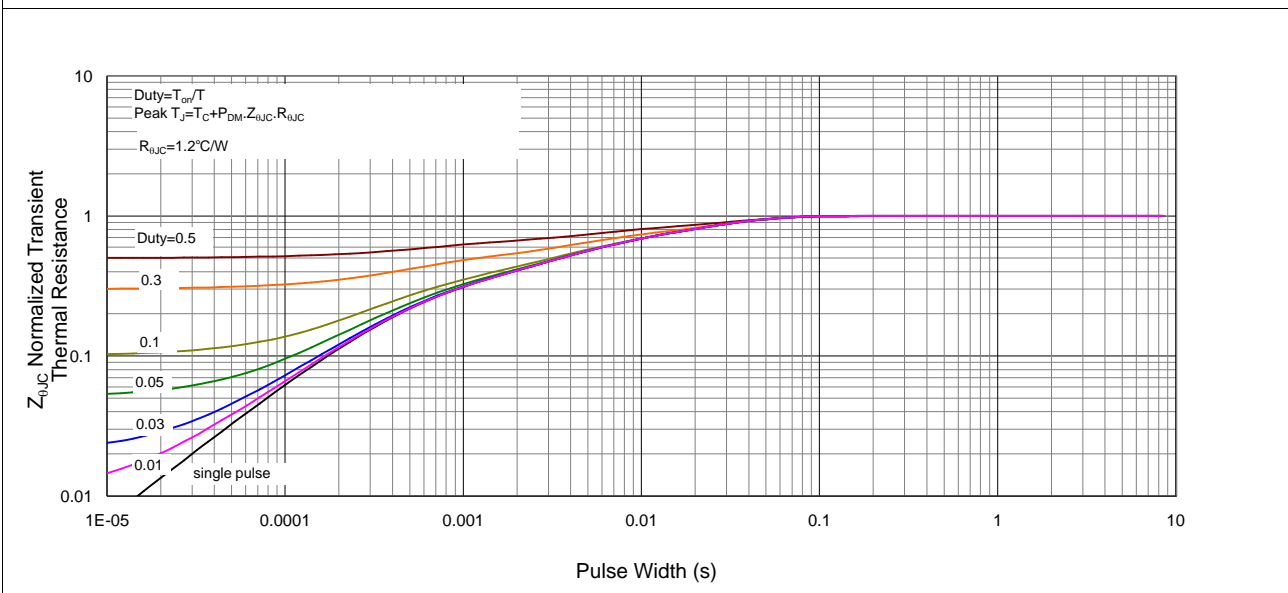
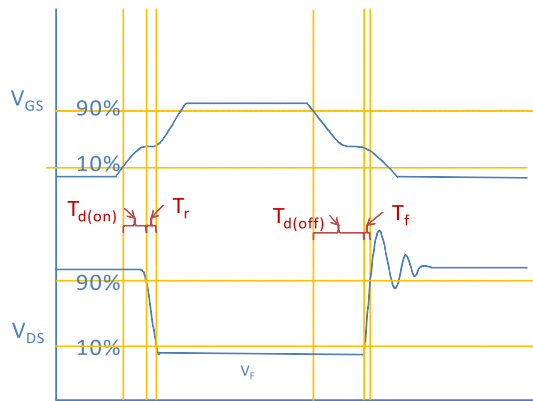
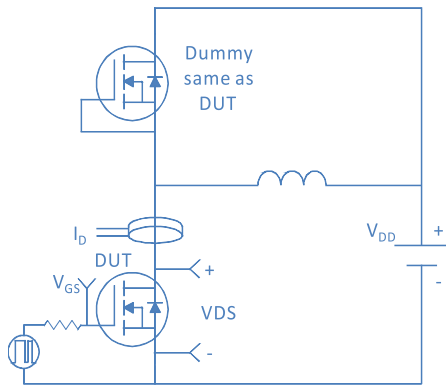


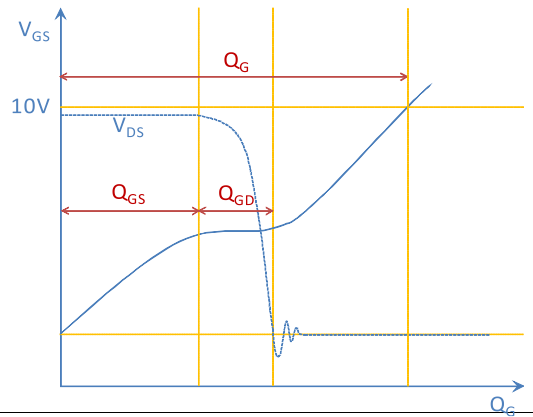
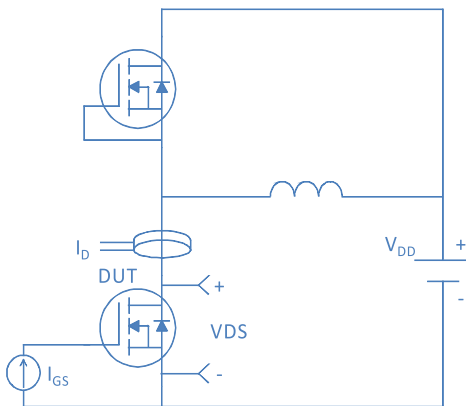
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



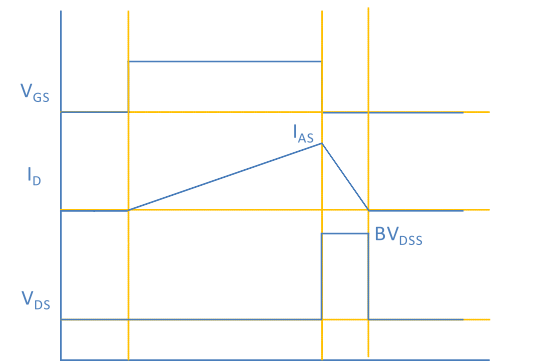
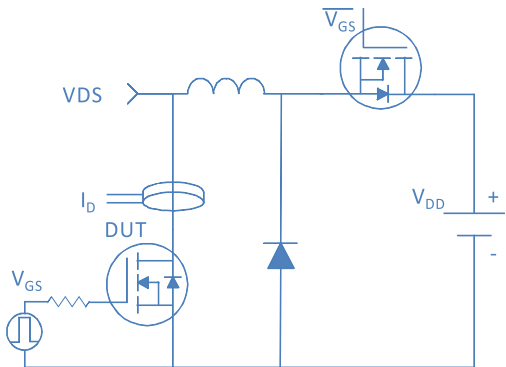
### Inductive switching Test



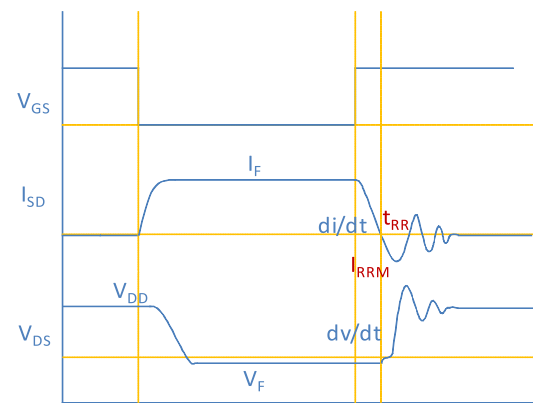
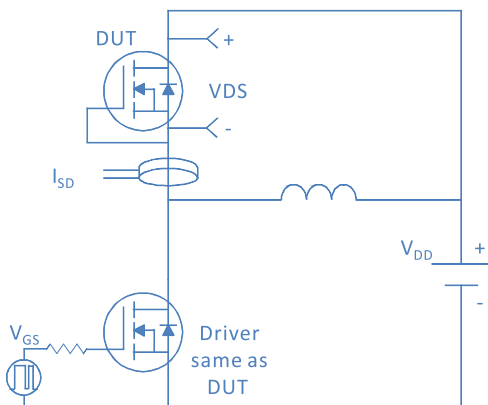
### Gate Charge Test



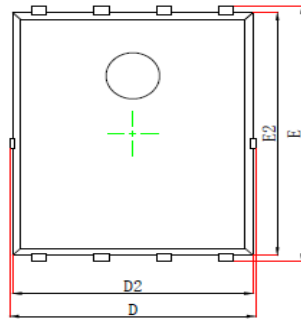
### Uclamped Inductive Switching (UIS) Test



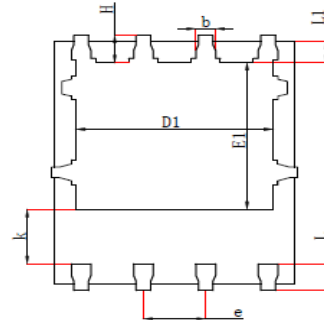
### Diode Recovery Test



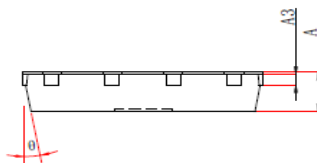
## DFN5x6\_P, 8 Leads



Top View  
[顶视图]



Bottom View  
[背视图]



Side View  
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254 REF		0.010REF	
D	4.680	5.120	0.184	0.202
E	5.900	6.126	0.232	0.241
D1	3.610	4.110	0.142	0.162
E1	3.380	3.780	0.133	0.149
D2	4.800	5.000	0.189	0.197
E2	5.674	5.826	0.223	0.229
k	1.100	1.390	0.043	0.055
b	0.330	0.510	0.013	0.020
e	1.270TYP		1.270TYP	
L	0.510	0.711	0.020	0.028
L1	0.424	0.576	0.017	0.023
H	0.410	0.726	0.016	0.029
θ	0°	12°	0°	12°